

# Cellular Telephone Power Converter

## FEATURES

- BiCMOS Low Power RF/Cellular Power Management
- Negative Supply Voltage at 5mA for GaAs MESFET Amplifiers
- Separate Micro-Power Logic Supply Enable
- Low Quiescent, 3mA, Operating Current
- Three Low Dropout (200mV) Regulators
- Power Good Indicator for Managing Power Supply Sequencing
- Low Power Mode Input Quiescent Current, 2 $\mu$ A (Max)
- Low Battery Early Warning Detection Output

## DESCRIPTION

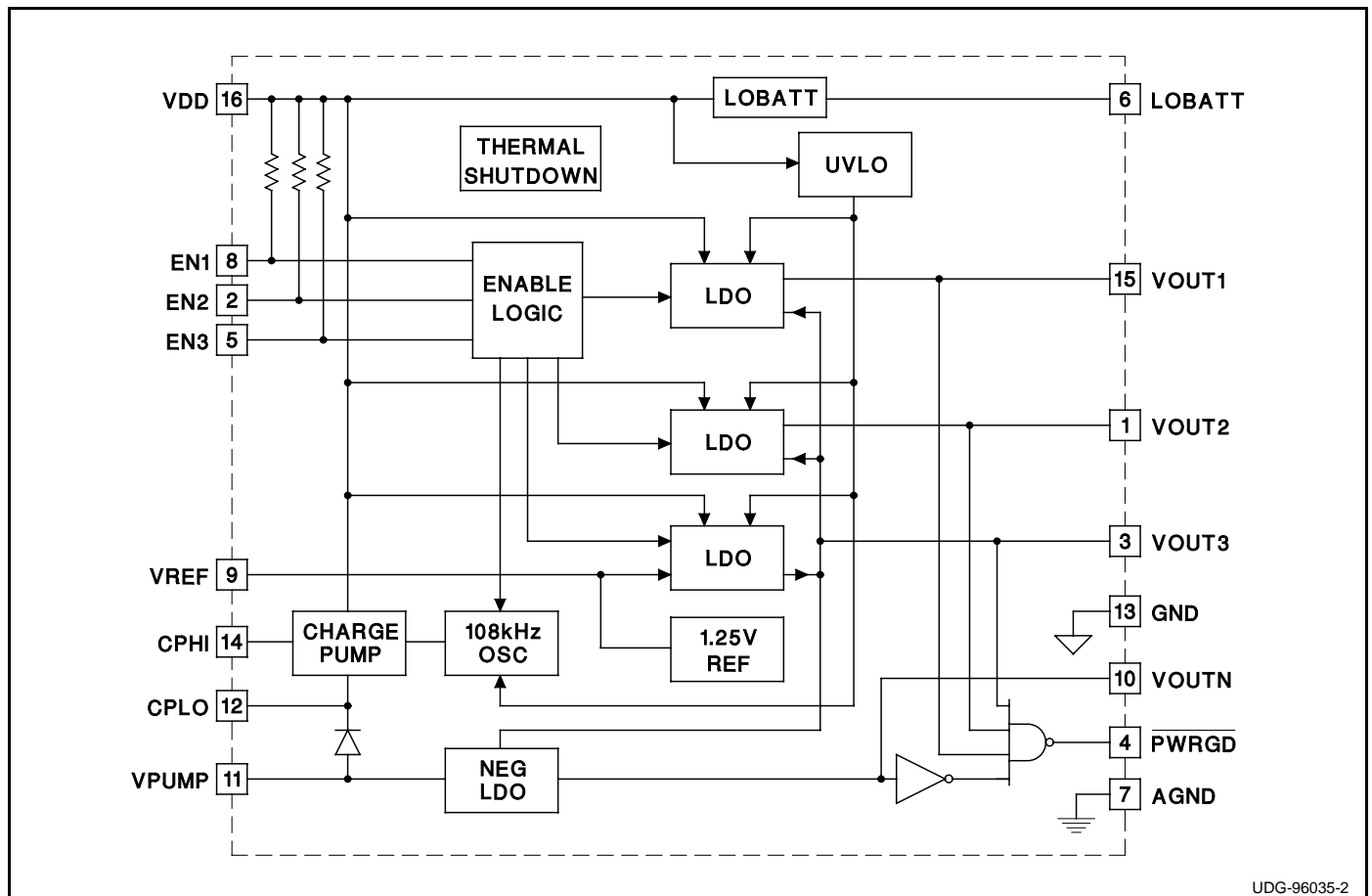
The UCC3930-3/-5 family of BiCMOS low power management controllers is designed for battery powered applications for RF/Cellular telephones, base stations, transmitters, receivers and pagers.

The circuit consists of three low dropout voltage regulators with <200mV maximum dropout, a low battery detection output, and a power good signal for managing power supply sequencing. Power management control is accomplished by the enable pins: EN1, EN2, and EN3 (See Table 1).

A negative supply for GaAs MESFET amplifiers is generated by a capacitive charge pump using a 0.1 $\mu$ F switching capacitor. The output noise of the negative supply is kept below 1mV by linearly regulating the coarse voltage present at the charge pump output.

Available packages include the 16-pin SSOP and 16-pin DIP. Consult Factory for exact SSOP-16 package dimensions.

## BLOCK DIAGRAM

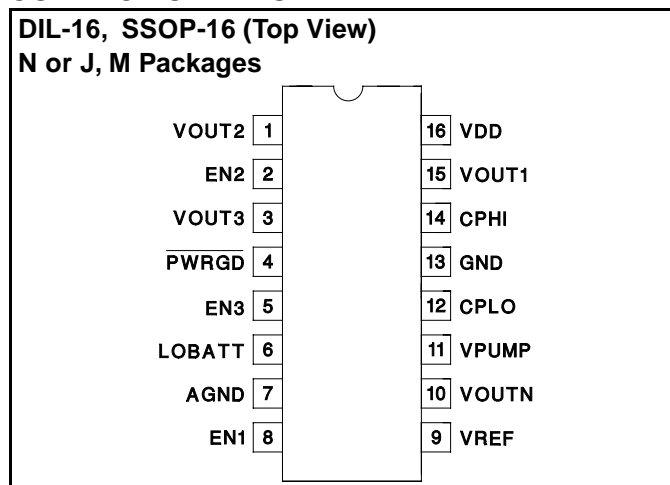


UDG-96035-2

### ABSOLUTE MAXIMUM RATINGS

Input Voltage (VDD) ..... +8V  
 EN Signal Voltage ..... -0.3V to VDD +0.3V  
 Regulator Output Current ..... 900mA  
 Storage Temperature ..... -65°C to +150°C  
 Junction Temperature ..... -55°C to +150°C  
 Lead Temperature (Soldering, 10 sec.) ..... +300°C  
*Currents are positive into, negative out of the specified terminal.  
 Consult Packaging Section of Databook for thermal limitations  
 and considerations of packages.*

### CONNECTION DIAGRAM



**ELECTRICAL CHARACTERISTICS** Unless otherwise specified,  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$  for UCC3930-3/-5 and  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$  for UCC2930-3/-5,  $C_{VPUMP} = 10\mu\text{F}$ ,  $C_P = 0.1\mu\text{F}$ ,  $C_{VOUT3} = C_{VOUTN} = 1.0\mu\text{F}$ ,  $C_{VREF} = 0.1\mu\text{F}$ ,  $C_{VDD} = 10\mu\text{F}$ ,  $C_{VOUT1} = C_{VOUT2} = 2.2\mu\text{F}$ ,  $3.5\text{V} < \text{VDD} < 8.0\text{V}$  for the UCC3930-3 and  $5.2\text{V} < \text{VDD} < 8.0\text{V}$  for the UCC3930-5, and EN1, EN2, and EN3 are 0V.  $T_A = T_J$ .

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
<b>Power Supply Section (UCC3930-3)</b>					
Shutdown Supply Current	EN1, EN2, EN3 = Open, $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$		2	10	$\mu\text{A}$
Low Power Operating Current	EN1 = 0V, EN2 and EN3 = Open		28	40	$\mu\text{A}$
VDD Operating Current	$I_{LOAD} = 0$ for All Outputs, EN1, EN2, EN3 = Low		3	4.5	mA
Undervoltage Lockout		3.0	3.2	3.4	V
<b>Regulator Section (UCC3930-3)</b>					
Output Voltage, VPUMP	$VPUMP_{LOAD} = 0\text{mA}$ , $VOUTN_{LOAD} = -5\text{mA}$ , VDD = 3.5V			-2.3	V
Output Voltage, VOUTN	$VPUMP_{LOAD} = 0\text{mA}$ , $VOUTN_{LOAD} = -5\text{mA}$	-2.7	-2.5	-2.3	V
Output Voltage, VOUT1, VOUT2	$I_{LOAD} = 0\text{mA}$ to 50mA	3.22	3.3	3.383	V
Output Voltage, VOUT3	$I_{LOAD} = 0\text{mA}$ to 5mA	3.22	3.3	3.383	V
	$I_{LOAD} = 0\text{mA}$ to 5mA, EN1 = Low, EN2 = EN3 = Open	3.135		3.465	V
LDO VOUT1 Current Limit (Peak)	VDD = 3.5V (Note 1)	-900	-500		mA
LDO VOUT2 Current Limit (Peak)	VDD = 3.5V (Note 1)	-900	-500		mA
LDO VOUT3 Current Limit	VDD = 3.5V	-180	-100		mA
VOUTN Current Limit			80	150	mA
VPUMP Output Resistance			150		$\Omega$
Oscillator Frequency			108		kHz
Low Battery Detector Threshold	Referenced to VOUT3	100	350	500	mV
<b>Power Supply Section (UCC3930-5)</b>					
Shutdown Supply Current	EN1, EN2, and EN3 = Open, $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$		2	10	$\mu\text{A}$
Low Power Operating Current	EN1 = 0V, EN2 and EN3 = Open		28	40	$\mu\text{A}$
VDD Operating Current	$I_{LOAD} = 0$ for All Outputs, EN1, EN2, EN3 = Low		3	4.5	mA
Undervoltage Lockout		4.15	4.65	5.15	V
<b>Regulator Section (UCC3930-5)</b>					
Output Voltage, VPUMP	$VPUMP_{LOAD} = 0\text{mA}$ , $VOUTN_{LOAD} = -5\text{mA}$ , VDD = 5.2V			-4.1	V
Output Voltage, VOUTN	$VPUMP_{LOAD} = 0\text{mA}$ , $VOUTN_{LOAD} = -5\text{mA}$	-4.6		-4.1	V
Output Voltage, VOUT1, VOUT2	$I_{LOAD} = 0\text{mA}$ to 50mA	4.875	5	5.125	V
Output Voltage, VOUT3	$I_{LOAD} = 0\text{mA}$ to 5mA	4.875	5	5.125	V
	$I_{LOAD} = 0\text{mA}$ to 5mA, EN1 = Low, EN2 = EN3 = Open	4.75		5.25	V
LDO VOUT1 Current Limit (Peak)	VDD = 5.2V (Note 1)	-900	-500		mA

**ELECTRICAL CHARACTERISTICS (cont.)** Unless otherwise specified, TA = 0°C to 70°C for UCC3930-3/-5 and -40°C to +85°C for UCC2930-3/-5, CVPUMP = 10µF, CP = 0.1µF, CVOUT3 = CVOUTN = 1.0µF, CVREF = 0.1µF, CVDD = 10µF, CVOUT1 = CVOUT2 = 2.2µF, 3.5V < VDD < 8.0V for the UCC3930-3 and 5.2V < VDD < 8.0V for the UCC3930-, and EN1, EN2, and EN3 are 0V. TA = TJ..

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
<b>Regulator Section (UCC3930-5) (cont.)</b>					
LDO VOUT2 Current Limit (Peak)	VDD = 5.2V (Note 1)	-900	-500		mA
LDO VOUT3 Current Limit	VDD = 5.2V	-180	-100		mA
VOUTN Current Limit			80	150	mA
VPUMP Output Resistance			150		Ω
Oscillator Frequency			108		kHz
Low Battery Detector Threshold	Referenced to VOUT3	100	450	650	mV
<b>Thermal Shutdown</b>					
Thermal Shutdown			165		°C
Thermal Shutdown Hysteresis			20		°C
<b>Power Management Section</b>					
Input Logic Low	Relative to GND			0.5	V
Input Logic High	Relative to VDD	VDD-0.5			V
Input Logic Pull-up Current	VDD = 8V	0.6	1.4	3	µA
Output Low Voltage	ILOAD = 0.1mA, Relative to GND			0.5	V
Output High Voltage	ILOAD = -0.1mA, Relative to VDD	VDD-0.5			V

Note 1: Once Thermal Cycling engages, the Average Current is much less in magnitude than this initial Peak Value.

## PIN DESCRIPTIONS

**AGND:** This is the analog ground for power outputs.

**CPhi, CPLO:** These pins are used to connect a flying capacitor, typically 0.1µF, across the two internal single-pole, double-throw switches. The internal switches provide a charge pumped voltage on the VPUMP pin.

**EN1, EN2, EN3:** These input pins control the operating mode of the device. Operation follows the truth table presented below.

**GND:** This is the ground return for all on-chip switching functions. Typically this pin is connected to the ground plane. The bypass capacitors connected to GND should have the shortest possible lead lengths.

**LOBATT:** A digital output signal that indicates a low battery condition when the VDD voltage approaches its'

minimum value required to maintain regulation. LOBATT is guaranteed to occur 100mV prior to the regulators dropping out of regulation. When only VOUT3 is enabled, LOBATT's output state is high.

**PWRGD:** This pin, when low, is a digital indication that all of the regulators which are enabled have exceeded 80% of their steady state output voltage. When only VOUT3 is enabled, PWRGD's output state is high.

**VDD:** Positive supply input for the regulator. Bypass this pin to GND with a 10µF low ESR, ESL capacitor.

**VOUT1, VOUT2, VOUT3:** These outputs are low dropout regulators with varying drive capabilities. They are internally short circuit current protected. The VOUT3 output is the primary reference for all supplies. This output is typically connected to non-switching loads such as bat-

EN1	EN2	EN3	VOUT1	VOUT2	VOUT3	VOUTN	VPUMP
0	0	0	ON	ON	ON	ON	ON
0	0	1	ON	OFF	ON	ON	ON
0	1	0	OFF	ON	ON	ON	ON
0	1	1	OFF	OFF	ON	OFF	OFF
1	0	0	NOT VALID				
1	0	1	NOT VALID				
1	1	0	NOT VALID				
1	1	1	OFF	OFF	OFF	OFF	OFF

### PIN DESCRIPTIONS (cont.)

tery back-up static RAM or low power analog circuitry. The 50mA regulators are output compensated with 2.2 $\mu$ F low ESR capacitors. The VOUT3 regulator is compensated with a single 1 $\mu$ F capacitor.

**VOUTN:** This pin is the power source for GaAs MESFET amplifiers. A single 1.0 $\mu$ F output capacitor connected to AGND will provide adequate loop compensation and filtering of the regulator.

**VPUMP:** This output is a coarsely regulated negative supply for preregulating the VOUTN GaAs MESFET supply. A single 2.2 $\mu$ F capacitor connected to GND will provide adequate filtering of the charge pump output.

**VREF:** This output is the internal 1.25V bandgap reference. The regulator is output compensated with a minimum 0.01 $\mu$ F capacitor. By utilizing external compensation, the reference voltage noise is kept to a minimum.

### APPLICATION INFORMATION

An application circuit for the UCC3930-3/-5 is shown in Figure 1. Careful attention must be paid to proper layout and decoupling techniques to insure low noise operation. The VDD and VPUMP pins should be bypassed di-

rectly to GND, while the output regulators and VREF should be separately bypassed to AGND. A single point connection should connect these two points as close to the IC as possible.

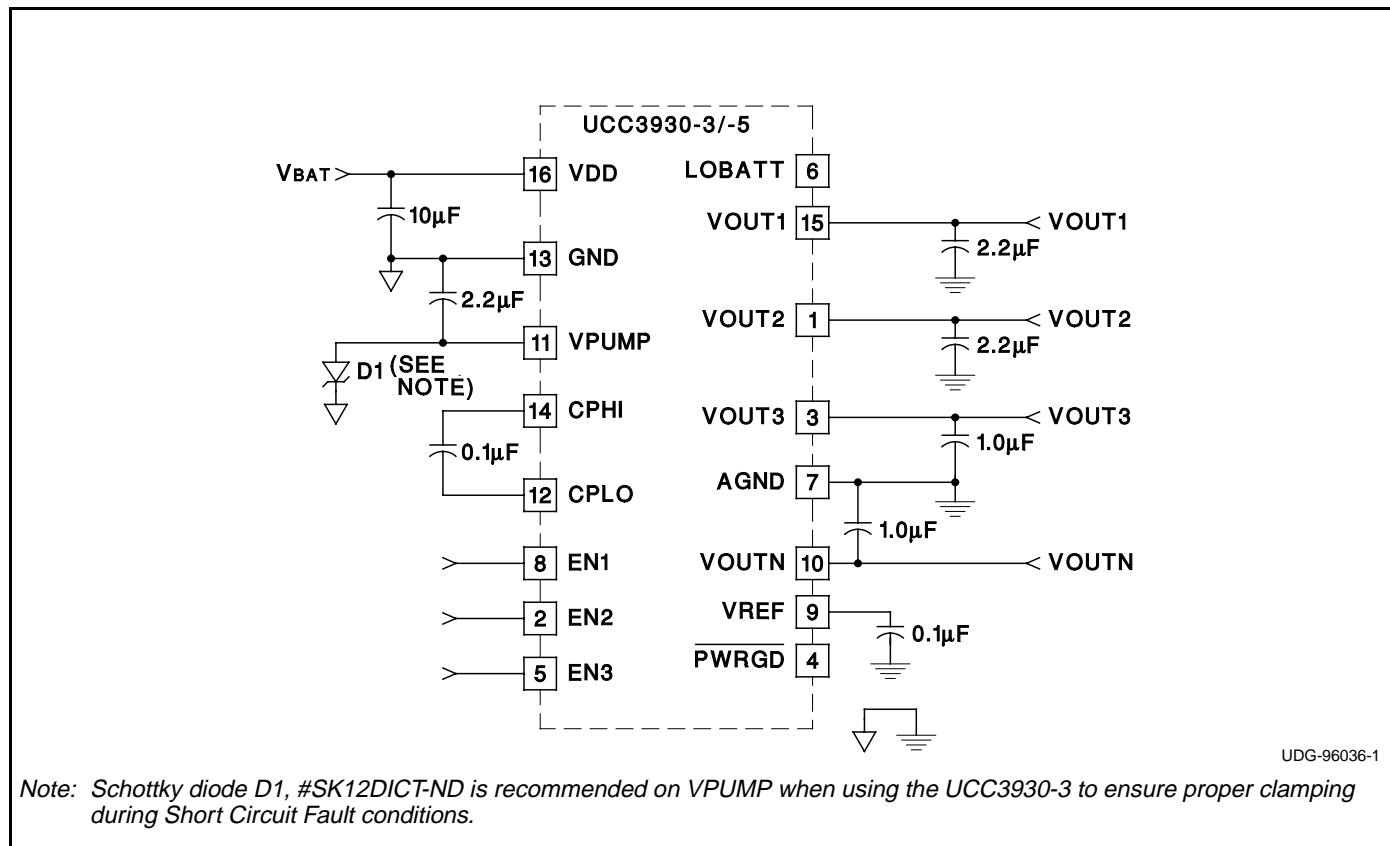
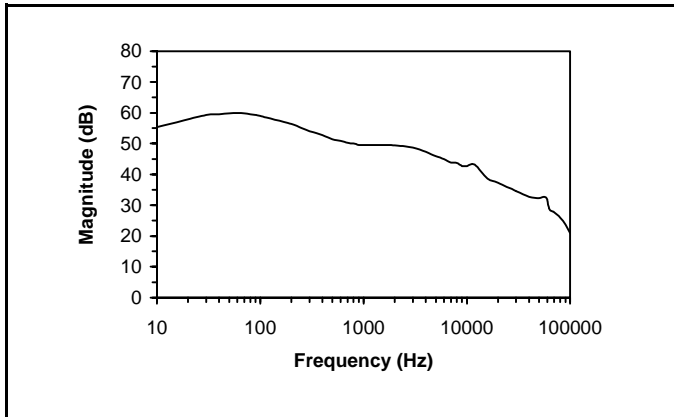
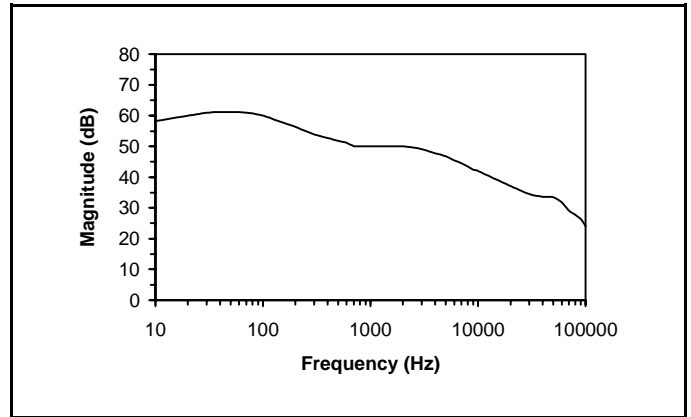


Figure 1. Typical Application Circuit

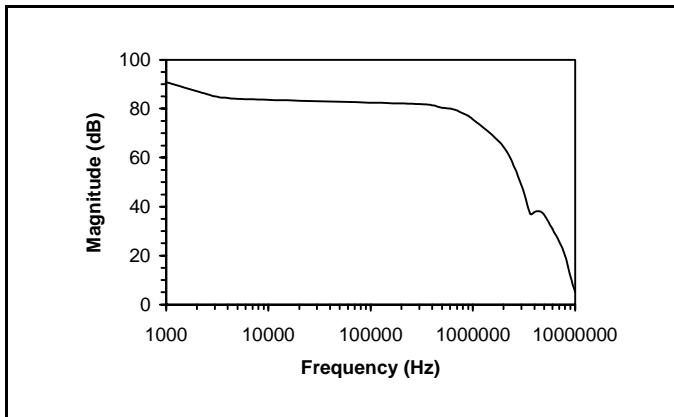
**TYPICAL CHARACTERISTICS**



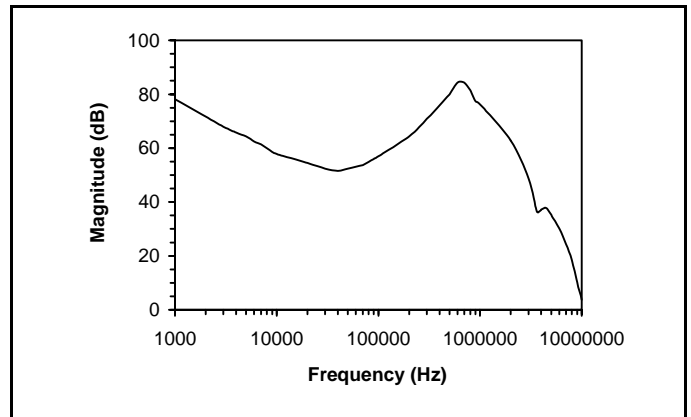
**Figure 2. Ripple Rejection: VDD to VOUT1 (VOUT2)  
Plot 1**



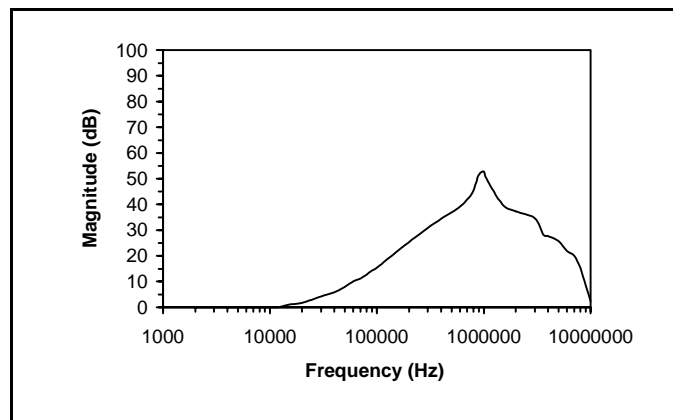
**Figure 3. Ripple Rejection: VDD to VOUT3  
Plot 2**



**Figure 4. Channel to Channel Noise Rejection:  
VOUT1 to VOUT2 (VOUT3)  
Plot 3**



**Figure 5. Channel to Channel Noise Rejection:  
VOUT2 to VOUT1 (VOUT3)  
Plot 4**



**Figure 6. Channel to Channel Noise Rejection:  
VOUT3 to VOUT1 (VOUT2)  
Plot 5**